# Proven Capability. High Speeds.

Building on the field proven capability of Teledyne DALSA's Xcelera frame grabber series, the Xtium™-CL MX4 is based on industry standard PCI Express™ Gen 2.0 expansion bus to deliver high speed access to host memory. The new Xtium series offers higher bandwidth to sustain Camera Link® 80-Bit modes over longer cable distances and supports a wide variety of area and line scan color/monochrome cameras, all in a compact, half-length, single slot solution.
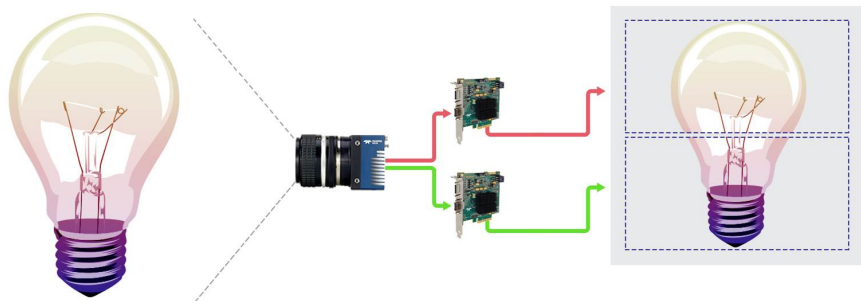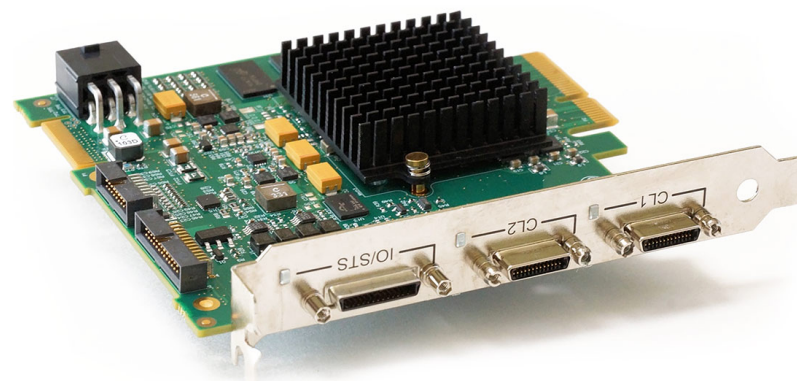
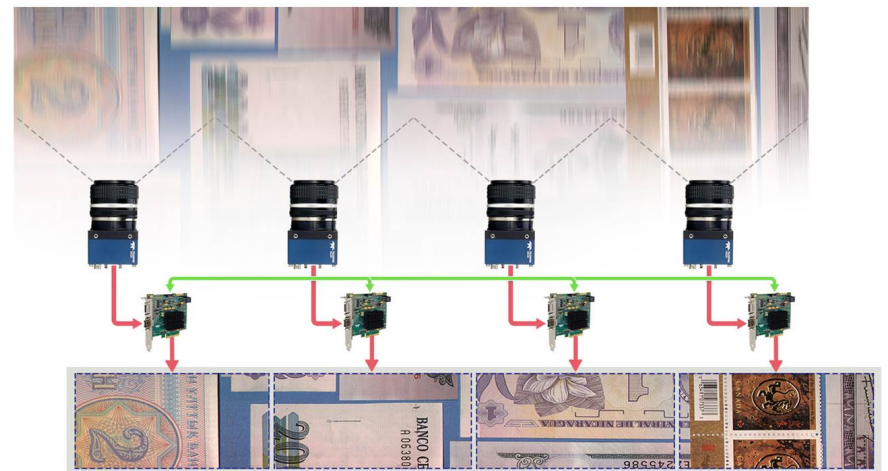# With great bandwidth comes great responsbility

The Xtium-CL MX4 takes full advantage of PCIe Gen 2.0 x4 platform to deliver a bandwidth in excess of 1.7 GB/s, while at the same time supporting PCIe Gen 1.0 slot to deliver 850 MB/s. The newly engineered, on-board, Data Transfer Engine (DTE) produces maximum bandwidth without the need for

specialized motherboards or chipsets. By enabling maximum sustained throughput and ready-to-use image data, the Xtium-CL MX4 minimizes CPU usage and improves processing times for the host applications. In addition, the Xtium series has been engineered with enhanced memory architecture allowing it to handle different sensor tap topologies while sustaining color decoding at the maximum frame/line rate.

Great features to make your job easier

The Xtium-CL MX4 offers built-in, robust electrical signals for external event synchronization, and status notification LEDs. One or more boards can be synchronized to acquire images from multiple area or line scan cameras simultaneously. The Xtium-CL MX4 supports Base, Medium, Full or 80-Bit mode Camera Link area and line scan, color and monochrome cameras with PoCL capabilities. And all Xtium-CL frame grabbers are built with Teledyne DALSA's **Trigger to Image Reliability** framework, which controls and monitors the entire process from trigger through image capture and transfer to host memory and helps protect you from data loss.

The Xtium series is engineered to meet the ever-increasing image resolution and faster frame rates of today's camera technology. So in addition to PCIe Gen 2.0 x4 and Camera Link, upcoming models will support Camera Link HS as well as other emerging interface standards on a PCIe Gen 2.0 x8

platform.

Specifications

Part Number	OR-Y4C0-XMX00
Board Type	PCIe
Host Bus	PCI Express Gen3 x8
Board Interface	Camera Link
Connectors	Data: 2 x SDR (mini Camera Link) Camera contro & GPIOs:1 x DH60-27pin on main bracket, 1 x 26-pin for internal connections Multi-board sync: 1 x 16 shrouded connector
Camera Format	2x Camera Link Base or 1x Camera Link Medium, Full or 80-bit (Deca)
Pixel Clock	20 to 85 MHz
Transmission Rate	85 MHz
Bits Per Pixel	8, 10, 12, 14 and 16-bit/pixel
Number of Camera Taps	1 Tap – 8/10/12/14/16-bit mono/bayer; 8/10/12-bit RGB 2 Taps – 8/10/12-bit mono/bayer; 8-bit RGB 3 Taps – 8/10/12-bit mono/bayer 4 Taps – 8/10/12-bit mono/bayer 64-bits:

8 Taps – 8-bit mono/bayer

Full packed 8-bit RGB/BGR/RGBY

80-bit:

8-Taps – 10-bit/pixel mono/bayer

10 Taps – 8-bit/pixel mono/bayer

Packed 8/12-bit RGB/BGR or

Packed 8-bit Bi-Color

Camera Control	External trigger input, strobe output, quadrature encoder input
GPIO	4 Opto-coupled inputs, usable as trigger inputs 8 LvTTL outputs, usable as strobe outputs
Frame Buffer	512 MB
Features	Power over Camera Link (PoCL), input lookup tables, flat-field/flat-line correction, bayer decoding, bi-color conversion, dead pixel (3 x 2) replacement, user programmable 3 x 3 convolution filter, metadata, strobe cycling/line-by-line
Software	Sapera LT SDK, Sapera Vision Software
OS Support	Windows 7 (32-bit)*, Windows 7 (64-bit)*, Windows 8 (32-bit), Windows 8 (64-bit), Windows 10 (32-bit), Windows 10 (64-bit), Linux (64-bit), WoW64 * Contact DALSA sales for more details
Input Camera Port	Up to 10-taps