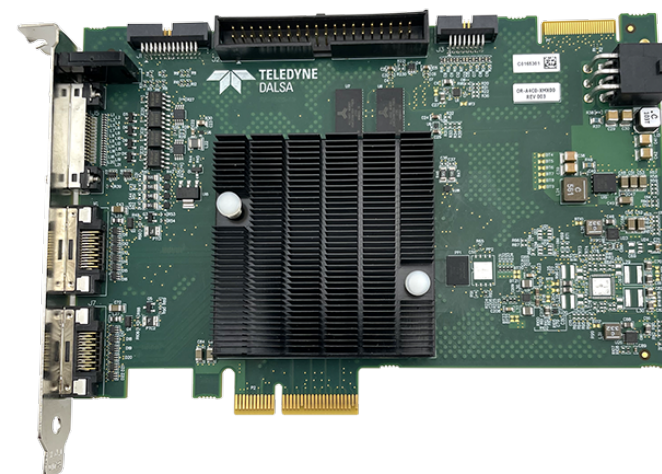


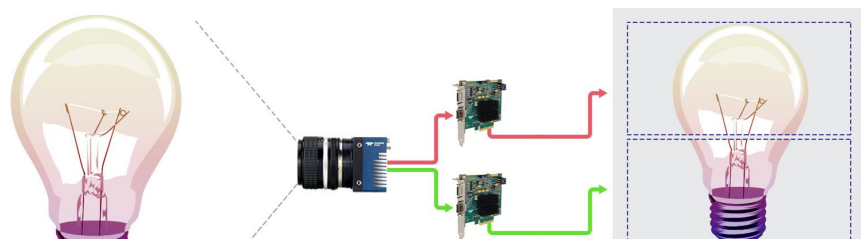
## Proven Capability. High Speeds. Full Compatibility.

Building on the field proven capability of Teledyne DALSA's Xtium™-CL MX4, the Xtium2™-CL MX4 supports Camera Link® standard and a wide variety of area and line scan color/monochrome camera configurations.



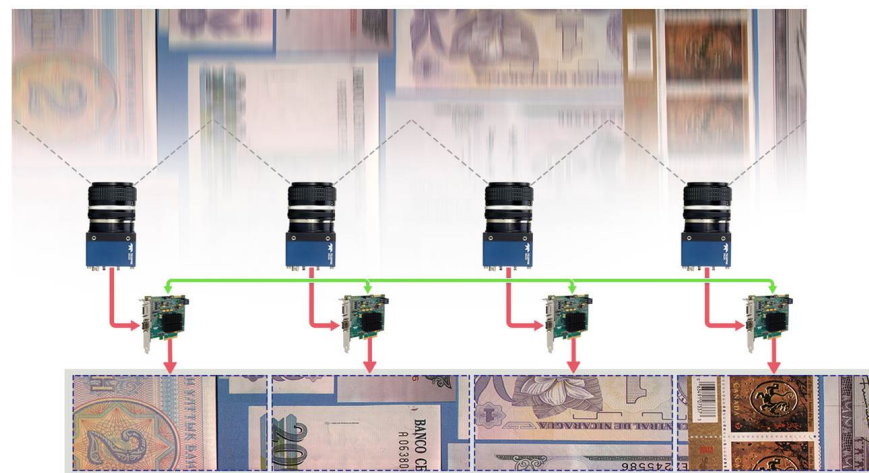
## With Great Bandwidth Comes Great Responsibility

The Xtium2-CL MX4 delivers sustained bandwidth more than 1.7 GB/s, while supporting PCIe Gen 3, 2 and 1 slots. Specifically designed to ease supply chain constraints, the Xtium2-CL MX4 has an identical feature set as the Xtium-CL

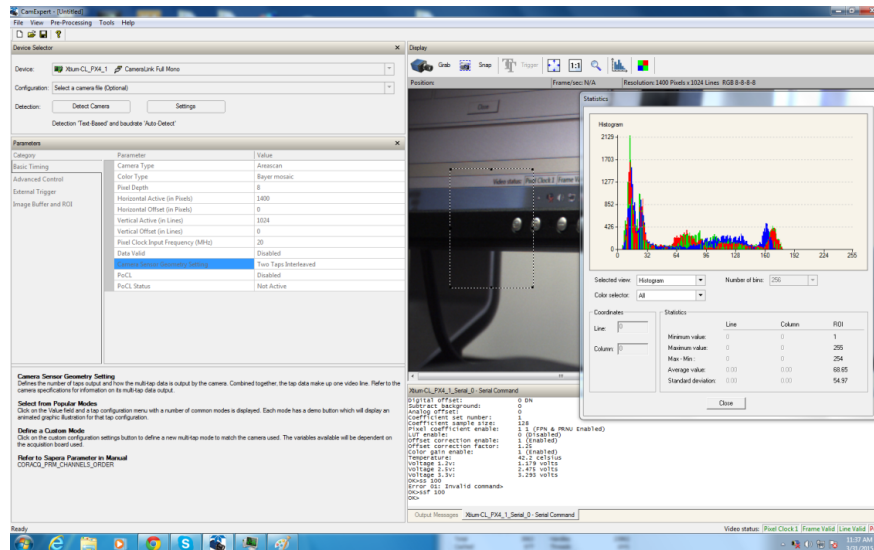


Teledyne DALSA's frame grabbers employ Trigger to Image Reliability framework to control and monitor the entire image capture process, from the trigger through to capturing and transferring images to the host memory. They also notify if any event and/or data loss occurs. As a leading supplier of machine vision components, Teledyne DALSA offers frame grabbers that comply with leading machine vision camera interface standards and supports its own and 3rd party

The proven on-board Data Transfer Engine (DTE) delivers maximum bandwidth with no specialized motherboards or chipsets. By enabling maximum sustained throughput and ready-to-use image data, the Xtium2-CL MX4 minimizes CPU usage and improves processing times for the host applications.



cameras.



## Free Acquisition and Control Software Libraries

The Xtium and Xtium2 series of frame grabbers are fully supported by **Sapera LT SDK**. Sapera LT SDK is an image acquisition and control software development toolkit (SDK) for Teledyne DALSA's cameras and frame grabbers. Hardware independent by nature, Sapera LT offers a rich development ecosystem for machine vision OEMs and system integrators. Sapera LT SDK supports image acquisition from cameras and frame grabbers based on standards including GigE Vision™, Camera Link®, CoaXPress®, and Camera Link HS™.

## Specifications

### Part Number

OR-A4C0-XXM00

### Bandwidth

Input Camera Link camera: up to 850 MB/s in frame grabber memory  
 PCIe bus output: up to 1.5 GB/sec sustained (PCIe payload @ 512 bytes)

### Board Type

PCIe

<b>Host Bus</b>	PCI Express Gen3 x8
<b>Board Interface</b>	Camera Link
<b>Connectors</b>	Data: 2 x SDR (mini Camera Link) camera control and GPIOs: 1 x DH60-27pin on main bracket 1 x 26-pin for internal connections multi-board sync: 1 x 16 shrouded connector
<b>Camera Format</b>	2 x Camera Link Base or 1 x Camera Link Medium, Full or 80-bit (Deca)
<b>Pixel Clock</b>	20 - 85 MHz
<b>Transmission Rate</b>	85 MHz
<b>Bits Per Pixel</b>	Mono: 8, 10, or 12-bit/pixel RGB: 8, 10 or 12-bit/pixel/color Bayer: 8, 10 and 12-bit/pixel Bicolor (RG,BG): 8-bit/color (line scan)
<b>Number of Camera Taps</b>	1 Tap - 8/10/12/14/16-bit mono/bayer; 8/10/12-bit RGB 2 Taps - 8/10/12-bit mono/bayer; 8-bit RGB 3 Taps - 8/10/12-bit mono/bayer 4 Taps - 8/10/12-bit mono/bayer, 64-bits: 8 Taps - 8-bit mono/bayer Full packed 8-bit RGB/BGR/RGBY 80-bit: 8 Taps - 10-bit/pixel mono/bayer 10 Taps - 8-bit/pixel mono/bayer Packed 8/12-bit RGB/BGR or Packed 8-bit Bi-Color
<b>Camera Control</b>	External trigger input, strobe output, quadrature encoder input
<b>GPIO</b>	4 Opto-coupled inputs, usable as trigger inputs 9 LvTTL outputs, usable as

**Frame Buffer**

strobe outputs

1024 MB on-board memory (shared with processing functions)

**Features**

Power Over Camera Link (PoCL), input lookup tables, flat-field/flat-line correction, bayer decoding, bi-color conversion dead pixel (3 x 2) replacement, user programmable 3 x 3 convolution filter, metadata, strobe cycling/line-by-line

**Software**

Sapera LT SDK

**OS Support**

Windows 11 (64-bit), Windows 10 (64-bit), Windows 10 (32-bit) through WOW64, Linux (64-bit)

**Input Camera Port**

Up to 2 cameras